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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,586	02/04/2004	Bumha Lee	50019.270US01/P05715	3798
23552	7590 03/09/2005		EXAM	INER
MERCHANT & GOULD PC			WILLIAMS, HOWARD L	
P.O. BOX 2903 MINNEAPOLIS, MN 55402-0903			ART UNIT	PAPER NUMBER
			2819	
			DATE MAILED: 03/09/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/771,586	LEE, BUMHA				
Office Action Summary	Examiner	Art Unit				
	Howard L. Williams	2819				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on						
,	— s action is non-final.					
	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ☐ Claim(s) 1-20 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-3 and 5-20 is/are rejected. 7) ☐ Claim(s) 4 is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)☐ The specification is objected to by the Examiner. 10)☒ The drawing(s) filed on <u>04 February 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>051704</u>. 	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

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The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The examiner acknowledges receipt of the information disclosure statement on 17 May 2004. An initialed copy of the citation form should accompany this letter.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The independent claims recite in the last couple of lines in each that the reference voltage and the sampled voltage are sampled at substantially the same time such that the reference voltage is pre-sampled in the pipelined converter. This phrasing seems a bit confusing due to connotations of "substantially at the same time" and "pre-sampled" and the proximity of the phrases without any pause producing punctuation. The pre-sampling of the reference and sampled voltage from the disclosure occur at the same time and for the claim to then say that reference is pre-sampled seems a little inconsistent. Perhaps the "pre-sampling" of the reference voltage is more in respect to the pipeline overall and could be separated to its own clause in the independent claims.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 15 and 18 are rejected under 35 U.S.C. 102(e) as anticipated by Opris (US 6,801,151 B1). Opris discloses a pipelined ADC and more particularly a revised structure of circuitry of the stages to shorten conversion time by overlapping

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operational phases of a stage of the pipeline. Figure 4 shows a sparse block diagram of the make-up of a stage in the pipeline, as apparent it includes sample and hold circuitry (410), comparator or evaluation circuitry (430), and a gain or MDAC section (420) which produces and supplies the residue signal to the next stage in the pipeline. Figure 5 shows a conversion stage circuitry in more detail while figure 6 provides a timing diagram of phased operation of the various stage components according to the phase of the clock signal. The comparator or evaluation stage (510) is illustrated as one comparator "triangle" for simplicity is parallel with the sample and hold stage represented by amplifier 520 and associated switched capacitor circuitry. The capacitor 512 in Opris serves as the sampling capacitor and feedback capacitor through the phased operation of the switches. The parallel arrangement of the comparator and sampling blocks such that both receive the stage input allows the comparison to take place at the same time as the sampling. The reference voltage Di * VREF (Di represents the comparator result and determines how VREF contributes to residue signal) to be fed to the gain/MDAC circuitry is available earlier.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-14, 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as unpatentable over Opris (US 6,801,151 B1) in view of Quinn (US 6,784,824 B1). Opris illustrated a single comparator so did not show 1.5 bit operation, the specific reference voltages applied to the comparators. Quinn illustrates, as applicants' prior art figures do also, 1.5 bit operation and reference voltages for the comparators -VREF/4 and VREF/4. It would have been obvious to combine Quinn and Opris to teach these features because overlapping bits (1.5 bit) from the stages of the pipeline provides error correction features thereby improving overall converter performance.

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Claim 4 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard L. Williams at telephone number (571) 272-1815.

3/4/05

Voice: (571) 272-1815

Howard L. Williams Primary Examiner

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